

Inter-chip Micro-connection Technology Driving System LSI for Hetero-function Integration

< Program for Fostering Regional Innovation (Global Type) >

Project Team

Project Manager

Tanemasa Asano
(Professor, Graduate School of Information Science and Electrical Engineering, Kyushu University)

Researcher

Naoya Watanabe
(Researcher, Fukuoka Industry, Science & Technology Foundation)

Enterprises

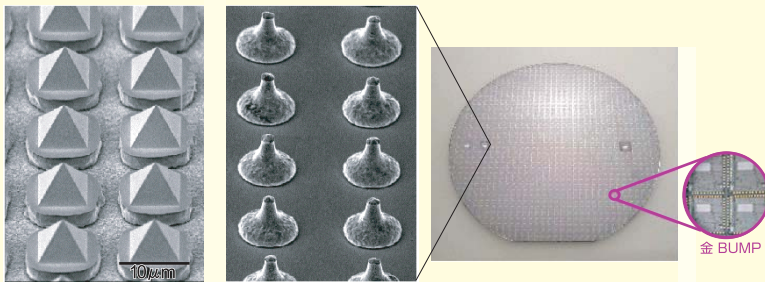
CASIO MICRONICS CO., LTD.

Purpose of the Research

In order to realize a high-performance and low power consumption system LSI in the future, a technology to integrate semiconductor into a multilayered structure is attracting a great deal of attention in all over the world. To develop the multilayered 3-dimensional architecture into a solution-providing system-LSI technology, an interconnection technology to increase the number of the signal transfer electrode between multilayered chips, which is currently about 2000 in the most advanced one, to tens of thousands or up to about one million must be developed. This research and development aims at developing a micro joining technology which can realize 3-dimensional architecture using Si-CMOS by utilizing the compliant bump electrode proposed by the representatives of the research. It also expected, due to the property of the compliant bump electrode, to realize integration of compound semiconductors and electronic functions using organic materials with Si-CMOS.

Outline of the Research

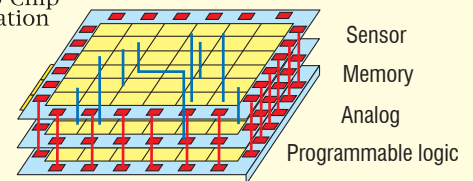
Compliant bump



It is able to install in anywhere, and any physical quantity can be computerized, visualized, made ready for networking.

A technology which is able to integrate any electronic function or electronic material.

Hetero-Chip Integration



RF communication chip

Results of the Research

● Number of electrodes connected

Currently, over ten thousand I/O connections between chips are possible for a chip.

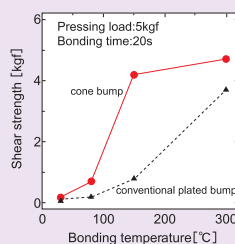
● Bonding temperature

Highly reliable connections can be made even at 150 degrees Celsius.

We have also developed a novel low-temperature bonding-technology which can make interconnection even at room temperature.

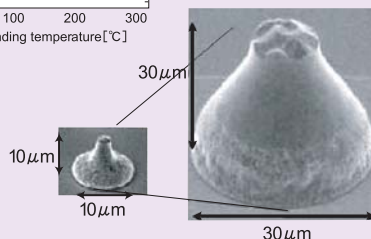
● Scalability

It is possible to manufacture electrodes in the range from 10 micron to over 30 micron according to applications.



(Left) Lower temperature bonding is possible. Even room temperature bonding became possible.

(Below) Various sizes of bumps are supported.



Prospective Fields of Application

It can greatly facilitate creation of new functions in system LSIs.

(Example)

- Portable terminal
- Supercomputer
- Flat-panel display
- Digital camera
- Sensor for medical or security purpose

and others



Information

Office
System LSI Division
FUKUOKA INDUSTRY, SCIENCE & TECHNOLOGY FOUNDATION
〒814-0001 3-8-33, Momochihama, Sawara-ku, Fukuoka City
Fukuoka Institute of System LSI Design Industry
TEL : +81 (92) 832 7155 FAX : +81 (92) 832 1700 <http://www2.lab-ist.jp/>



Information

Cooperative support organization
Knowledge Cluster Division, Industry-Academia Cooperation Department,
Industry-Academia Cooperation Center
Kitakyushu Foundation for the Advancement of Industry, Science and Technology
〒808-0135 2F, Industry-Academia Cooperation Center
Kitakyushu Science and Research Park
2-1, Hibikino, Wakamatsu-ku, Kitakyushu City, Fukuoka
TEL : +81 (93) 695 3440 FAX : +81 (93) 695 3439 <http://www.ksrp.or.jp/fa/s/>