R&D of High-Yield Platform for LSI Circuits

<Program for Fostering Regional Innovation (Global Type) >

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Purpose of the Research

Yield loss due to multiple factors such as design errors, manufacture defects, and test failures of integrated circuits has become such a serious problem that it deeply threatens the semiconductor industry. In order to solve this problem, a cluster consisting of members from universities, testing houses, IT companies, and semiconductor manufactures has been formed to develop innovative technologies for high-precision fault diagnosis technology, low-power test generation, test program automatic verification, knowledge-based test failure analysis and test computation speed-up. The ultimate goal is to establish an effective yield improvement platform for semiconductor integrated circuits. This platform will help improve the competitive strength of the Japanese semiconductor industry.

Summary of the Research

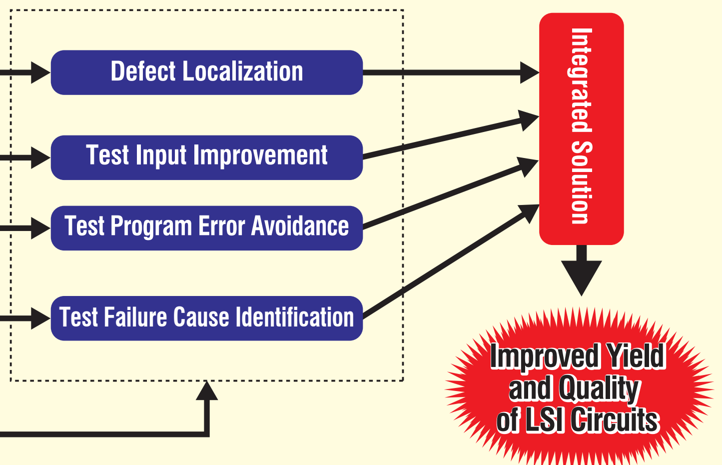
High-Precision Fault Diagnosis Technology
- Extended X-fault model for modeling timing-related defects
- High-resolution diagnosis method for structure and timing defects

Low-Power Test Generation Technology
- Test generation for reducing power supply noise in at-speed scan testing

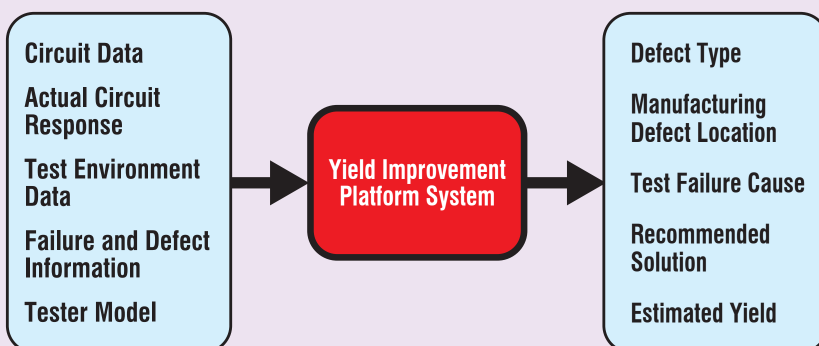
Test Program Automatic Verification Technology
- Computer-aided test program generation
- Tester-acquired-data-based test program verification

Knowledge-Based Test Failure Analysis Technology
- Knowledge analysis and modeling of test yield analysis
- Rule base construction for test failure analysis
- High-speed inference engine for test failure analysis and feedback

Test Computation Speed-Up Technology
- Test-application-specific parallel and distributed processing



Final Research Goals



Prospective Fields of Application

- High-resolution LSI failure analysis
- Efficient test failure analysis
- Expert-level solution recommendation
- Yield analysis and estimation

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Semiconductor manufacturers
Fables makers
Foundries
Testing houses
Failure analysis firms

Information

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