

R&D of System Integration Platforms

<Program for Fostering Regional Innovation (Global Type) >

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Purpose of the Research

●Development of MEMS compatible SiP design tool

We will develop a three-dimensional System-In-a-Package (SiP) design tool including the Micro electro mechanical Systems (MEMS) device to be able to design the overall package.

●Development of a next-generation mounting technology evaluation technology

We will develop Test Element Group (TEG) and Reference Substrate (RS) which are able to evaluate the process to mount an advanced device such as a 90 nm node die. Moreover we will establish technologies to mount a MEMS device and a high-frequency SiP.

●Deployment of SIPOS in Asia

We will deploy the activity of SIPOS (System Integration Platform Organization Standard) in Asia, which was organized to standardize the high-density substrate used in the System-in-a-Package (SiP) and others, and will construct Asia's semiconductor integration platform in Fukuoka.

Summary of the Research

We aim at developing an EDA tool required to design and develop SiP including MEMS devices in a short time, and establishing SiP evaluation technologies.

●Development of MEMS device design tool

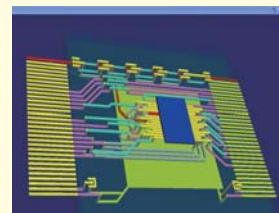
We will add the stress analysis technology to the SiP design tool, and develop a tool which is able to simulate the MEMS device characteristic under stress and able to design the whole SiP including MEMS device.

●Establishment of evaluation technologies

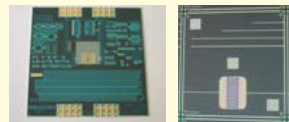
We will develop TEG and RS which are able to evaluate the mounting process of advanced device using low-k materials. And we will establish evaluation methods which support technologies such as COG, device-embedded substrate, and silicon interposer.

●SIPOS activity

In order to share design database, evaluation methods, failure analysis database, we will provide design tool, TEG and RS, and aim to construct a semiconductor integration platform in Asia. And we will develop and standardize new technologies such as device-embedded substrate.



Example of a component-contained board designed with the developed tool



RS (left) of the developed SIPOS and TEG(right) which is mounted on it

Results of the Research (Fiscal year 2007)

●Development of SiP design tool which is able to perform stress analysis

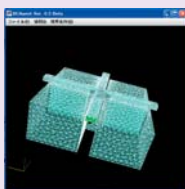
The MEMS design tool ver. 1.0 was completed in March 2008 which is the result of adding a stress analysis function to the three-dimensional SiP design tool (STEERSIP) developed in the Intelligent Cluster Creation Project (1 stage).

●Development of advanced TEG and RS

In order to evaluate the assembling process, we developed an advanced TEG, which uses low-k materials, and RS, upon which the TEG is mounted. We also developed glass TEG and RS for evaluating Chip-on-Glass (COG) and device-embedded substrate.

●Evaluation of electrical property under stress

We realized a design which takes into consideration of residual stress within a package by evaluating the MOSFET's DC characteristic and high frequency characteristic when stress is being applied by four-point bending apparatus, and comparing them with the simulation results.



Example of stress analysis result

Prospective Fields of Application

- Design and development of MEMS and SiP in a short period of time
- Failure analysis in advanced device mounting process
- Evaluation of stress characteristics of a high-frequency device

Cooperation with other institutions

- We provided TEG of SIPOS to EPADs consortium in Japan Institute of Electronics Packaging(JIEP).
- We are promoting international collaboration research with Fraunhofer IZM (Germany), IMEC (Belgium), and ITRI (Taiwan).



Information

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Information

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