R&D of Digital Cinema Streaming System over Wireless Mesh Network

<Program for Fostering Regional Innovation (Global Type) >

Project Team

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Enterprises

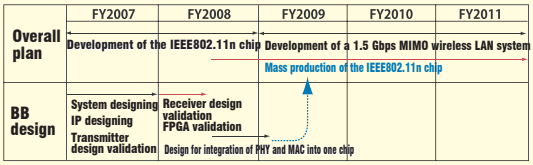
Radrix Co., Ltd./Ricoh Co., Ltd. /Logical Product Corporation

Development of a Chip for IEEE802.11n: 1 Development of PHY/MAC layer

The MIMO technology is a technology which is able to improve greatly the transmission speed and transmission quality in wireless communication with a limited frequency bandwidth in comparison to the conventional single antenna (SISO: Single Input Single Output) system by installing multiple antennas for the transmitter and receiver to form multiple spatio-temporal channels (transmission path) between the transmitter and receiver.

Figure 4 shows the configuration example of the receiver using the MIMO technology.

1. Development schedule

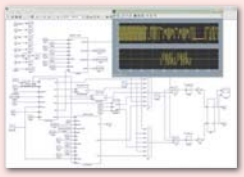


2. Development specification

Item	Designed model 1	Designed model 2
MCS	0 - 15	0 - 32
Antennas	2	4
Subcarriers	52 / 56	52 / 56 / 114
Packet mode	Legacy packet, Mixed packet	
Bandwidth	20MHz	20MHz / 40MHz
FEC	BCC	Two BCCs
Etc	Short G.I.	
Data rate	- 144Mbps	- 600Mbps
System clock	80MHz	

Specification of Designed Models

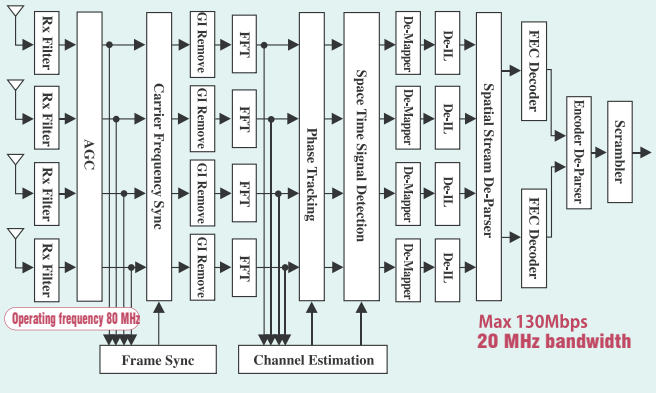
3. Example of logic synthesis validation



■IEEE802.11n PHY layer RTL synthesis result
Device:ALtera Stratix2

4. Obtained results

IEEE802.11n compatible PHY system
- Receiver RTL design model -



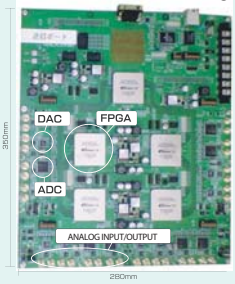
Developed IP

IP	Logic elements	Operating frequency
Frame Sync.	24003	88MHz
Carrier Sync.	34875	106.6MHz
Co-CIC(MMSE)	14069	153.1MHz
Channel Estimation	727	215.9MHz
FFT,IFFT	2036	87.7MHz
LDPC	90000	-
ETC.	-	Over 80MHz
11n Transmitter	23591	92.7MHz

MAC Design specification

Throughput	> 100Mbps
Packet Mode	Legacy and Mixed for IEEE 802.11n
Data bus width	32bit
Access Protocol	Distributed coordination function(DCF) HCF contention-based channnel access (EDCA)
Network Architecture	MAC for station in infrastructure QoS Basic Service Set
Network Management	Centralized synchronization and passive scanning TS operation for QoS Traffic TXOP operation Block Ark operation

■FPGA board for validating MIMO system



Design specification for FPGA board

Number of gates	Ten million or more gates by converting it into the number of gates
A/D, D/A converter	210MHz, 12 bits 8 units each
Interface	Gigabit Ethernet (No number) Supports ZF, MMSE, V-BLAST, GLST, and STBC
System clock	200MHz
Development IP set	
Reference (Matlab m file)	IEEE802.11a, IEEE802.11n, IEEE802.15 TG3a
Error correcting circuit	Viterbi,LDPC
MIMO interference elimination	ZF,MMSE,V-BLAST, GLST, STBC(16)
Synchronization circuit	Frame synchronization, carrier synchronization
IP details	
Viterbi	Supports 11a, 11n
LDPC	Supports 11n draft ver.1
STBC・SDM	Supports up to 4x4
Frame synchronization	FI synchronization circuit (Antenna combined type)
Carrier synchronization	Auto-correlation carrier synchronization circuit (Antenna combined type)
FFT/IFFT	radix4 IFFT, FFT Supports 64-128 points

■MIMO-RF module

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